Application No. 10/082,771
Filed: February 25, 2002
TC Art Unit: 2633
Confirmation No.: 4427

Amendments to the Specification

References to paragraph numbers are taken from the official publication hereof (Publication No. 2004/0208527).

Please replace paragraph [0065] with the following amended paragraph.

[0065] Turning now to the drawings, reference is made to Fig. 1, which is a high level diagram of a section 10 of a data communications network having an end-to-end connection, which is constructed and operative in accordance with a preferred embodiment of the invention. A section of a communications network 12 is shown. At a ~~path level 14~~ path level, The network elements of the network 12 are represented by terminating equipment 16 and digital cross-connect 18, which can multiplex and demultiplex a payload. A protection switching arrangement is provided, using two lines 20, 22. The network 12 may be a SONET network, an SDH network, an Ethernet network, an MPLS network, or other digital communication network. System interfaces occur throughout the network 12, and many types of equipment can be used as network

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elements. System interface 24 and system interface 26 are shown representatively.

Please replace paragraph [0072] with the following amended paragraph.

[0072] In the counter sections 46, 48, 50, the counter 52 and the counter 54 accumulate data ~~of the primary~~ through the primary port 40 the secondary port 44 respectively under control of the processor 30. The counter 56 is also controlled by the processor 30, and accumulates data that is received via the primary port 40 or via the secondary port 44, whichever is currently connected by the switch 64. Preferably, the counters are implemented in software, and the associations between the counters and the ports, and switching operations are realized by addressing or suppression of addressing of the counters by the processor 30 in accordance with program instructions.

Please replace paragraph [0073] with the following amended paragraph.

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[0073] The processor 30 is linked to a data memory 66, in which associations with the counter sections 46, 48, 50 and the various counters 52, 54, 56 are accessed using an interface index 68. The interface index 68 can be maintained in an information model, such as a management information database (MIB) in the case of a simple network management protocol (SNMP). The value held in the counter 56 is represented as a virtual index. Typically, the counter section 46 counts performance related primitives, for example, ES. Then the data counted by the counter 52 represents the ES on the primary channel 38, and the data counted by the counter 54 represents the ES on the secondary channel 42. Both are indexed by the interface index 68. The value of the counter 56 represents the ES on the active channel.

Please replace paragraph [0101] with the following amended paragraph.

[0101] Reference is now made to Fig. 5, which is a flow chart illustrating an alternative embodiment of step 72 (Fig. 3). The procedure of Fig. 5 is similar to Fig. 4, in which like reference numbers denote the same elements. However, following

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completion of step 114, accumulation of data in the hardware registers 60, 62 is continued for the duration of the current read interval. All data accumulating during the current read interval, subsequent to the switchover that was detected in decision step 84, is accumulated in the reassigned counters. ~~Control then returns immediately to decision step 88.~~ This embodiment has the advantage of greater precision, at the cost of more complex control requirements.

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